REMARKS

This paper is responsive to the Office Action mailed July 11, 2006. Claims 1, 2, 4-8, 10, 14 and 15 are pending in this application. Claims 1, 2, 4-8, 10, 14 and 15 have been amended. Support for all amended claims can be found in the specification, and no new matter has been added by these amendments. Reconsideration of the claims in view of the amendments and the following remarks is respectfully requested.

Examiner Interview

Applicants thank the Examiner for her time on January 8, 2007 to discuss the proposed claim amendments and clarification of certain differences between the proposed claims and the cited prior art references.

Claim Rejections under35 U.S.C. § 102

Claims 1, 2, 4-8, 10, 14, and 15 stand rejected under 35 U.S.C. § 102(a) as being anticipated by admitted prior art, specification at pages 2-4 and Figure 1. Applicants respectfully traverse the rejection.

The claimed invention relates to automatically setting temporary inspection conditions when inspecting a semiconductor device. The temporary inspection conditions are automatically set based on a received product name of the semiconductor device and a received process name by which the semiconductor device is to be inspected. The temporary inspection conditions may include an inspection area of the semiconductor device, an alignment pattern of the semiconductor device, a spacial filter associated with the semiconductor device, or an area of the semiconductor device to be excluded.

Claim 1, as amended, recites in part "receiving a product name of a semiconductor device to be inspected and a process name that identifies a process by which the semiconductor device is to be inspected." [page 6, lines 16-17; Fig. 1]. Claim 1 also recites "accessing a design database to down load design information associated with the semiconductor device, wherein the design information is identified using the received product name and the

received process name." [page 6, line 18; Fig. 2]. Claim 1 further recites "processing the down loaded design information to set temporary inspection conditions, wherein the temporary inspection conditions comprise at least one of an inspection area of the semiconductor device, an alignment pattern of the semiconductor device, a spacial filter associated with the semiconductor device, or an area of the semiconductor device to be excluded." [page 6, lines 19-20 and 32-35; Fig. 2].

The "admitted prior art" describes manually setting the inspection condition. The admitted prior art does not disclose the elements of claim 1. Specifically, the admitted prior art does not disclose, "accessing a design database to down load design information associated with the semiconductor device, wherein the design information is identified using the received product name and the received process name; [and] processing the down loaded design information to set temporary inspection conditions." Thus, claim 1 is allowable.

Independent claims 4, 7 and 14 have also been amended to recite, "accessing a design database to down load design information associated with the semiconductor device, wherein the design information is identified using the received product name and the received process name; [and] processing the down loaded design information to set temporary inspection conditions." Thus, claims 4, 7 and 14 are allowable.

Claims 2, 5, 6, 8, 10 and 15 depend from one of the independent claims discussed above and are allowable at least for the same reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 206-467-9600.

Respectfully submitted,

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